WHAT IS CLAIMED IS:

1. A high-frequency signal suppresser, comprising:

a resister having a first terminal serving as an input terminal of said high-frequency signal suppresser;

a first capacitor having a first terminal electrically connected to a high voltage source and a second terminal electrically connected to a second terminal of said resister;

a second capacitor having a first terminal electrically connected to said first capacitor and said resister, and a second terminal electrically connected to a low voltage source; and

a shaping circuit having an input terminal electrically connected to said first capacitor, said resister, and said second capacitor, and an output terminal serving as an output terminal of said high-frequency signal suppresser;

wherein a high-frequency signal inputted from said input terminal of said high-frequency signal suppresser is filtered by said resister, said first capacitor, and said second capacitor, and then shaped by said shaping circuit so as to generate a logic signal at said output terminal of said high-frequency signal suppresser.

2. The high-frequency signal suppresser according to claim 1, wherein said resister is one selected from a group consisting of an output resistance of a complementary metal-oxide-semiconductor, a metal-oxide-semiconductor resister, a transmission gate, a poly-Si, and a quantum well.

3. The high-frequency signal suppresser according to claim 1, wherein said first capacitor and said second capacitor are one of an input parasitic capacitor of said shaping circuit and a metal-oxide-semiconductor capacitor.

4. The high-frequency signal suppresser according to claim 1, wherein said shaping circuit is one selected from a group consisting of a SCHMITT trigger circuit, a logic gate, and a comparator.

5. A high-frequency signal suppresser, comprising:

a filter having an input terminal; and

a shaping circuit having an output terminal and electrically connected in series with said filter;

wherein a high-frequency signal inputted from said input terminal is filtered by said filter and then shaped by said shaping circuit so as to generate a logic signal at said output terminal.

6. The high-frequency signal suppresser according to claim 5, wherein said filter is a low pass filter.

7. The high-frequency signal suppresser according to claim 5, wherein said filter comprises:

a resister having a first terminal serving as said input terminal and a second terminal electrically connected to said shaping circuit;

a first capacitor having a first terminal electrically connected to a high voltage source and a second terminal electrically connected to said resister and said shaping circuit; and

a second capacitor having a first terminal electrically connected to said first capacitor, said resister, and said shaping circuit, and a second terminal electrically connected to a low voltage source.

8. The high-frequency signal suppresser according to claim 7, wherein said resister is one selected from a group consisting of an output resistance of a complementary metal-oxide-semiconductor, a metal-oxide-semiconductor resister, a transmission gate, a poly-Si, and a quantum well.

9. The high-frequency signal suppresser according to claim 7, wherein said first capacitor and said second capacitor are one of an input parasitic capacitor of said shaping circuit and a metal-oxide-semiconductor capacitor.

10. The high-frequency signal suppresser according to claim 5, wherein said shaping circuit is one selected from a group consisting of a SCHMITT trigger circuit, a logic gate, and a comparator.